## AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 48. (Cancelled)

49. (Previously Presented) An integrated circuit comprising:

a first insulating layer disposed between a substrate and a first metal layer;

a trench defined by a recess in the first insulating layer, the trench not extending below a top surface of the substrate;

a first contact pillar extending substantially from the top surface of the substrate to a bottom surface of the first metal layer within the trench; and

a capacitor formed in the trench overlying the first contact pillar such that the capacitor is formed at least in part on a side of the first contact pillar, and the first contact pillar is a first plate of the capacitor.

50. (Original) The integrated circuit of claim 49, further comprising a second contact pillar extending substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer, wherein the second contact pillar is substantially the same height as the first contact pillar.

51. (Original) The integrated circuit of claim 49, wherein the capacitor comprises a storage element of a memory cell.

52. (Original) The integrated circuit of claim 51, wherein a storage node of the storage element comprises the first contact pillar.

53. (Original) The integrated circuit of claim 52, wherein the storage node further comprises a conducting layer lining the trench and the side of the first contact pillar.

54. (Previously Presented) The integrated circuit of claim 50, wherein the second contact pillar is a bit line contact pillar.

55-56. (Cancelled)